**R15**

**Code No: 123BU**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**B. Tech II Year I Semester Examinations, February - 2024**
**SWITCHING THEORY AND LOGIC DESIGN**
**(Electronics and Communication Engineering)**

**Time: 3 Hours** **Max. Marks: 75**

**Note:** i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

## PART - A
**(25 Marks)**

| | | |
|---|---|---|
| 1.a) | What is the need for error detecting code? | [2] |
| b) | Convert $(B0F9.0EB)_{16}$ to binary. | [3] |
| c) | Give significance of Don't Care. | [2] |
| d) | Give brief about prime implicants. | [3] |
| e) | Define latch. | [2] |
| f) | How does race around condition eliminated? | [3] |
| g) | What is sequential circuit? | [2] |
| h) | What are the types of counters and give brief of anyone. | [3] |
| i) | Define finite state machine. | [2] |
| j) | Write short notes on Mealy state machine. | [3] |

## PART - B
**(50 Marks)**

2.a) Discuss about Binary Coded Decimal code and its properties.
b) Simplify the following function and implement it with NOR gates [4+6]
$F = \overline{AC} + ACE + AC\overline{E} + \overline{A}C\overline{D} + \overline{A}D\overline{E}$.

**OR**

3.a) Why a NAND and NOR gates are known as universal gates?
b) Simplify the following Boolean expressions using the Boolean theorem and realize universal logic gates. [2+8]
(A+B+C) (B′+C) + (A+D) (A′+C).

4.a) Discuss about tristate bus System.
b) Minimize the following expressions using K-map and realize using NAND logic. [3+7]
F = ∑ m (1,3,5,8,9,11,15) +d (2,13)

**OR**

5.a) Simplify the following function in sum of products using don't care conditions.
$F = \overline{W}X(\overline{Y}Z + Y\overline{Z}) + WYZ$.
b) Discuss about Tabular Method. [6+4]

6. Design a clocked T-Flip flop with neat diagram and truth table and explain the operation. [10]

**OR**

7.a) Write the procedure of conversion from one type of flip-flop to another.
b) What is the timing and triggering consideration? [5+5]

8.a) Compare and contrast Ripple counter and ring counter.
b) Draw and explain sequential circuit state diagram with suitable example. [4+6]

**OR**

9.a) With a neat diagram, explain the operation of ring counter using shift register.
b) Discuss the approaches to design of synchronous sequential finite state machines. [5+5]

10.a) Discuss the capabilities and limitations of finite state machines.
b) Explain the ASM technique to design a sequential circuit. [5+5]

**OR**

11.a) With neat block diagram, explain Moore model.
b) Briefly explain about system design using data path and control subsystems. [5+5]

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